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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,321	03/06/2002	Makoto Kanbe	1035-371	7734

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EXAMINER
NGUYEN, JIMMY H

ART UNIT	PAPER NUMBER
2673	19

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DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,321	KANBE ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,20,23,31,33,41 and 45-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18,20,23,31,33,41 and 45-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/974,496* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) __ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 12/22/2003 (entered into the file wrapper as Paper No. 18). Claims 18, 20, 23, 31, 33, 41 and 45-49 are currently pending in the application. An action follows below:

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature, "a source enable signal output circuit", lines 24-25 of claim 18, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 18, 20, 23, 31, 33, 41 and 45-48 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding to claims above, the disclosure, when filed, does not contain sufficient information regarding to the claimed feature, "said power source control circuit comprising a

source enable signal output circuit outputting to said source driver control circuit a source enable signal ... period", of independent claim 18, lines 24-26. The disclosure, specifically fig. 13 and the description at page 40, lines 8-19, teaches a power source control circuit 56 for outputting a source enable signal 70 to the source driver control circuit 54. However, a source enable signal output circuit is not found in the original disclosure.

5. It is suggested Applicants to change "said power source control circuit comprising a source enable signal output circuit", lines 24-26 of claim 18, to -- said power source control circuit --, in order to overcome the above drawing objection and the above rejection under 35 USC 112, first paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 49 is rejected under 35 U.S.C. 102(b) as being anticipated by Yasui et al. (USPN: 5,248,963), hereinafter Yasui.

Regarding to claim 49, the claimed invention reads on Yasui as follows: Yasui discloses an erasing device for a LCD device (fig. 3) having a LCD panel (10) whose pixels are driven by active elements (13), for erasing a display image on said LCD panel when a power source of a main body of said LCD device is turned off, the erasing device comprising power source OFF detecting circuit (a voltage drop detector 24, fig. 5, abstract) for detecting the turning off of the power source of the main body of LCD device, a power source control circuit (a circuit including

elements 22, 23, 25, 26, 27 and an inherent circuit for providing signals D, PCK and M, see figs. 3 and 5) including a power holding circuit 22 for maintaining power to the LCD panel for a certain period after the power source is turned off (col. 4, lines 50-53), and an erasing circuit (a circuit including elements 16, 17 and an inherent opposing electrode circuit for providing a signal to a common electrode 12b, figs. 3 and 5) for applying an OFF-level voltage (a voltage level corresponding to pixel data D of logic "0", col. 3, lines 58-60), using the power supplied by the power holding circuit 22 of the power source control circuit, to all pixels in the LCD panel, thereby erasing the display in a short time after the turning OFF of the power supply (figs. 3 and 5, col. 3, lines 1-22 and lines 58-67). As noting in fig. 3, Yasui further discloses the LCD panel including a pixel electrode (12a), an opposing electrode (12b) and an inherent liquid crystal material therebetween. Yasui further teaches that the erasing circuit applies to both the pixel electrode (12a) and the opposing electrode (12b) an OFF-level voltage (the common potential EG of zero volt, col. 1, lines 58-59) within time T and a negative voltage E2 latter (col. 1, lines 58-60 and col. 6, lines 3-9). In other words, the rectangular wave signal having amplitudes of negative voltage E2 and common potential EG of zero volt is expressly taught by Yasui. Accordingly, the Yasui reference anticipates this claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 18, 20, 23, 31, 33, 41 and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui and further in view of Tsuboyama et al. (USPN: 5,592,191, cited in IDS filed on 03/06/2002), hereinafter Tsuboyama.

Regarding to claims 18, 20, 23 and 45, the claimed invention reads on Yasui as follows: Yasui discloses an erasing device for a LCD device (fig. 3) having a LCD panel (10) whose pixels are driven by active elements (13), for erasing a display image on said LCD panel when a power source of a main body of said LCD device is turned off, the erasing device comprising power source OFF detecting circuit (a voltage drop detector 24, fig. 5, abstract) for detecting the turning off of the power source of the main body of LCD device, a power source control circuit (a circuit including elements 22, 23, 25, 26, 27 and an inherent circuit for providing signals D, PCK and M, see figs. 3 and 5) including a power holding circuit 22 for maintaining power to the LCD panel for a certain period after the power source is turned off (col. 4, lines 50-53), and an erasing circuit (a circuit including elements 16, 17 and an inherent opposing electrode circuit for providing a signal to a common electrode 12b, figs. 3 and 5) for applying an OFF-level voltage (a voltage level corresponding to pixel data D of logic "0", col. 3, lines 58-60), using the power supplied by the power holding circuit 22 of the power source control circuit, to all pixels in the LCD panel, thereby erasing the display in a short time after the turning OFF of the power supply (figs. 3 and 5, col. 3, lines 1-22 and lines 58-67). Yasui further discloses the erasing circuit including a source driver (a source bus driver 16b, best seen fig. 1), a source driver control circuit (a circuit including a plurality of shift registers 16a, fig. 1), for providing signals to control the source driver (16b), and an inherent opposing electrode control circuit for outputting an opposing electrode signal (a voltage) to opposing electrodes (common electrodes 12b) (fig. 3,

col. 3, lines 58-67). Yasui further teaches the power source control circuit (a circuit including elements 22, 23, 25, 26, 27 and an inherent circuit for providing signals D, PCK and M, see figs. 3 and 5) including a source enable signal output circuit, for controlling the source driver control circuit (16a) and the opposing electrode control circuit. Yasui further teaches the erasing circuit applying to both the pixel electrode (12a) and the opposing electrode (12b) an OFF-level voltage (the common potential EG of zero volt, col. 1, lines 58-59) within time T and a negative voltage E2 latter (col. 1, lines 58-60 and col. 6, lines 3-9). In other words, the rectangular wave signal having amplitudes of negative voltage E2 and common potential EG of zero volt is expressly taught by Yasui. Accordingly, the Yasui reference discloses all the claimed subject matter except that the Yasui source enable signal output circuit does not output to the source driver control circuit (16a) a source enable signal which is at a selecting level during the certain period T.

However, Tsuboyama discloses a related erasing device for a LCD, the power source control circuit (a circuit including elements 104 and 105, see fig. 1) comprising a source enable signal output circuit including a logic control unit 107, for outputting a source enable signal (data side Vc control signal, fig. 1), which is at a selecting level during the certain period TE (fig. 5A), to the source driver control circuit (shift register/latch circuit 25, fig. 2) which, in response to the source enable signal, to cause the source driver (a circuit including switching array 22, fig. 2) to provide a voltage V4 to the pixel electrode, thereby turning off the LCD (fig. 5A, col. 4, lines 37-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the logic control unit 107 in the source enable signal output circuit of Yasui because this would allow the source enable output circuit controlling the source driver control circuit and the source driver, for applying the OFF voltage during a certain period

after the turning off of the power, thereby eliminating image disturbance from a display panel even when power is turned off, and enabling uniform orientation of the liquid crystal, as taught by Tsuboyama (col. 1, line 64 through col. 2, line 27).

Regarding to claims 31 and 33, Yasui fails to teach the active matrix type LCD device including a reflective LCD device or a Guest-Host LCD device. Official Notice is taken that the active matrix type LCD device including a reflective LCD device or a Guest-Host LCD device is notoriously well known and expected in the art. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have the active matrix type LCD device of Yasui including a reflective LCD device and a Guest-Host LCD device as these displays are known to consume less power since these displays operates without using a backlight.

Regarding to claims 41, 46 and 47, as discussed above, Yasui teaches the erasing means outputting a voltage signal (E2) to both pixel electrode (12a) and opposing electrode (12b), by means of the source driver (16b) and the opposing electrode signal control circuit (fig. 3, col. 3, line 58 through col. 4, line 16). Yasui further discloses the erasing means including a gate driver (a gate bus driver 19) for outputting a gate driving signal (outputs G1, G2, ..., Gm), which turns on gate lines (15_1-15m) sequentially to turn on the active elements (TFTs 13) per line and a gate driver control circuit (a circuit including elements 18 and 20) (see fig. 4) for receiving a gate enable signal (a clear signal CL, fig. 4), as a starting signal for the gate driver, so that a gate driving signal (G1, ..., Gm) is outputted to gate lines (15_1-15m) (see figs. 2 and 4).

Regarding to claim 48, Yasui further discloses that, during the erasing period (T), the gate driving signal (G1, G2, ..., Gm) is fixed at a high level (col. 4, lines 3-11).

Response to Arguments

10. With respect to claim 49, pages 9-11, applicants state that Yasui does not disclose rectangular wave signal being applied by the LCD erasing means, pages 11-13, examiner disagrees. Yasui, at column 6, lines 3-6, expressly teaches "The display electrode 12a and the counter electrode 12b (the latter being supplied with the voltage E2) are both supplied with the common potential within the time Y", i.e., the rectangular wave signal having amplitudes of negative voltage E2 and common potential EG of zero volt.

11. Applicant's arguments with respect to claims 18, 20, 23, 41 and 45-48, pages 11-17, have been considered but are moot in view of the new ground(s) of rejection. See the new ground (s) of rejection above.

12. Further, it is noted Applicants that Applicants' arguments should address the "**current**" Office Action, e.g., Applicants state "The Action states that "a capacitor (25), a resistor (26), ... and a voltage VB correspond to the source driver control circuit, and the source enable signal respectively", page 13, lines 8-10, which is not stated in the last Office Action dated 10/21/2003. Furthermore, Applicants state "Yasui does not disclose a feature in which "source enable signal output circuit" generates a "source enable signal" that is inputted to the source driver control circuit during a predetermined period after the power source is turned OFF", page 12, last line through page 13, line 2, as discussed in the last Office Action, examiner indicated that the above underlined feature is disclosed by the Tsuboyama reference, but not in the Yasui reference. See the last Office Action dated 10/21/2003, page 7, last 3 lines, and the rejection above.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is (703) 306-5422. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at (703) 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

JHN
February 29, 2004

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600